Technical Datasheet

Graphene Field-Effect Transistor Chip: S31/20nm

General Description

The GFET-S31/20nm chip from Graphenea provides 30 top-gated graphene devices distributed in a grid pattern on the chip. All the 30 devices have a 3-probe geometry, leveraging Graphenea's proprietary High-K Metal Gate (HKMG) process flow to provide a top-gate with an EOT = 20nm. This scheme allows for individual control of the conductance of each of the graphene channels within the die. There are 3 graphene channel dimensions to allow investigation of size dependence on device properties, enabling immediate optimization.

Because the whole device is passivated, even the graphene channel, it shows exceptional Dirac point stability and low-hysteresis; this is of great advantage specially in the fields of AC/RF electronics, optoelectronics and photonics. Moreover, the device can be operated under a double-gate configuration, using both the global back-gate and the local top-gate.

Features	Applications

- Local gating enables individual device control.
- Aggresive dielectric scaling via HKMG allows for low-power operation (<5V)
- Encapsulated devices, highly stable Dirac point + low hysteresis
- 30 individual GFETs per chip, with different sizes for optimization
- Mobilities typically in excess of 600 cm^2/V·s

- Graphene device research
- Optoelectronics
- Photodetectors
- Photonics
- Optical modulators
- Biosensors

Typical Specifications

Chip dimensions	10 mm x 10 mm
Chip thickness	525 μm
Number of channels per chip	30
Gate Oxide thickness (EOT)	20 nm
Gate Oxide material	Al_2O_3
Dielectric breakdown	> 13 kV/mm
Metallization	Au contacts
Graphene field-effect mobility	> 600 cm^2/V·s
Dirac point	< 5 V
Yield	> 75 %

Absolute Maximum Ratings

Maximum gate-source voltage	± 5 V
Maximum temperature rating	150 °C
Maximum drain-source current density	10^7 A·cm^{-2}

GFET-S30 Layout
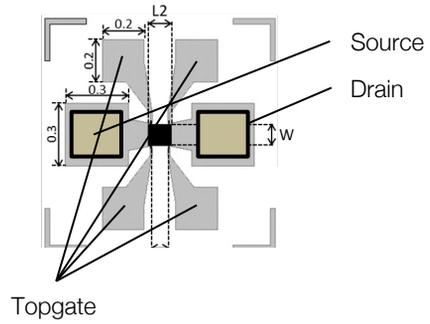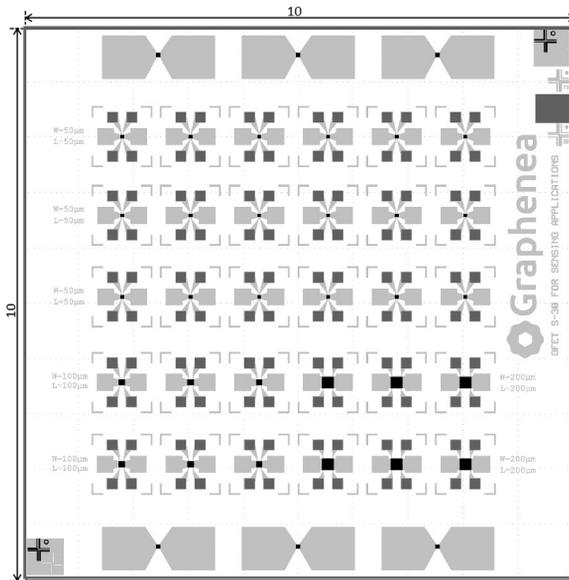
Channel geometries

Description	W (µm)	L1 (µm)	L2 (µm)	QTY
Small	50	30	50	18
Medium	100	75	100	6
Large	200	175	200	6

Device cross-section
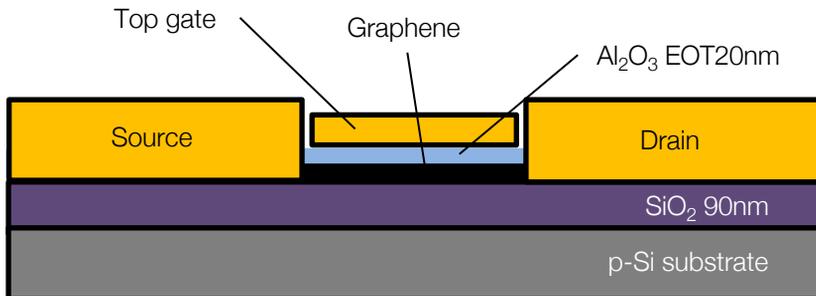
Typical characteristics
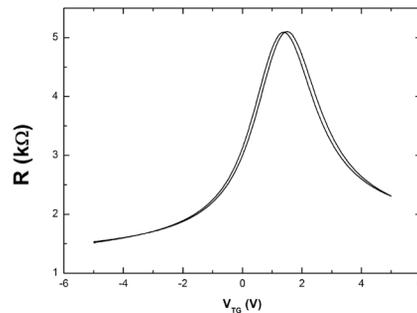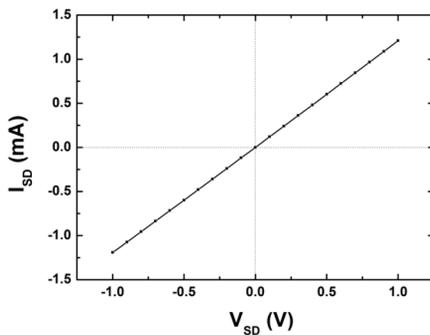
Output curve (left) and transfer curve measured at source-drain voltage of 20mV (right), measured at room temperature and ambient conditions on a device with W=L=50 µm.

Dirac point & hysteresis drifts
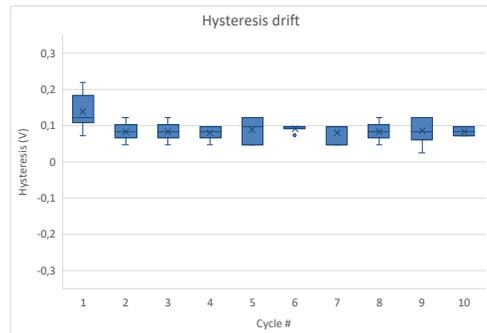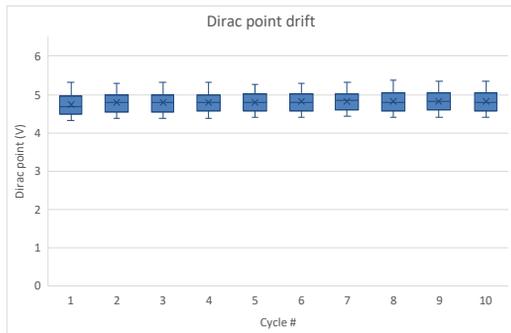
Dirac point drift (left) and hysteresis drift (right) when the gate voltage is swept up to 10 times (voltage sweep= |5|V, N=10).